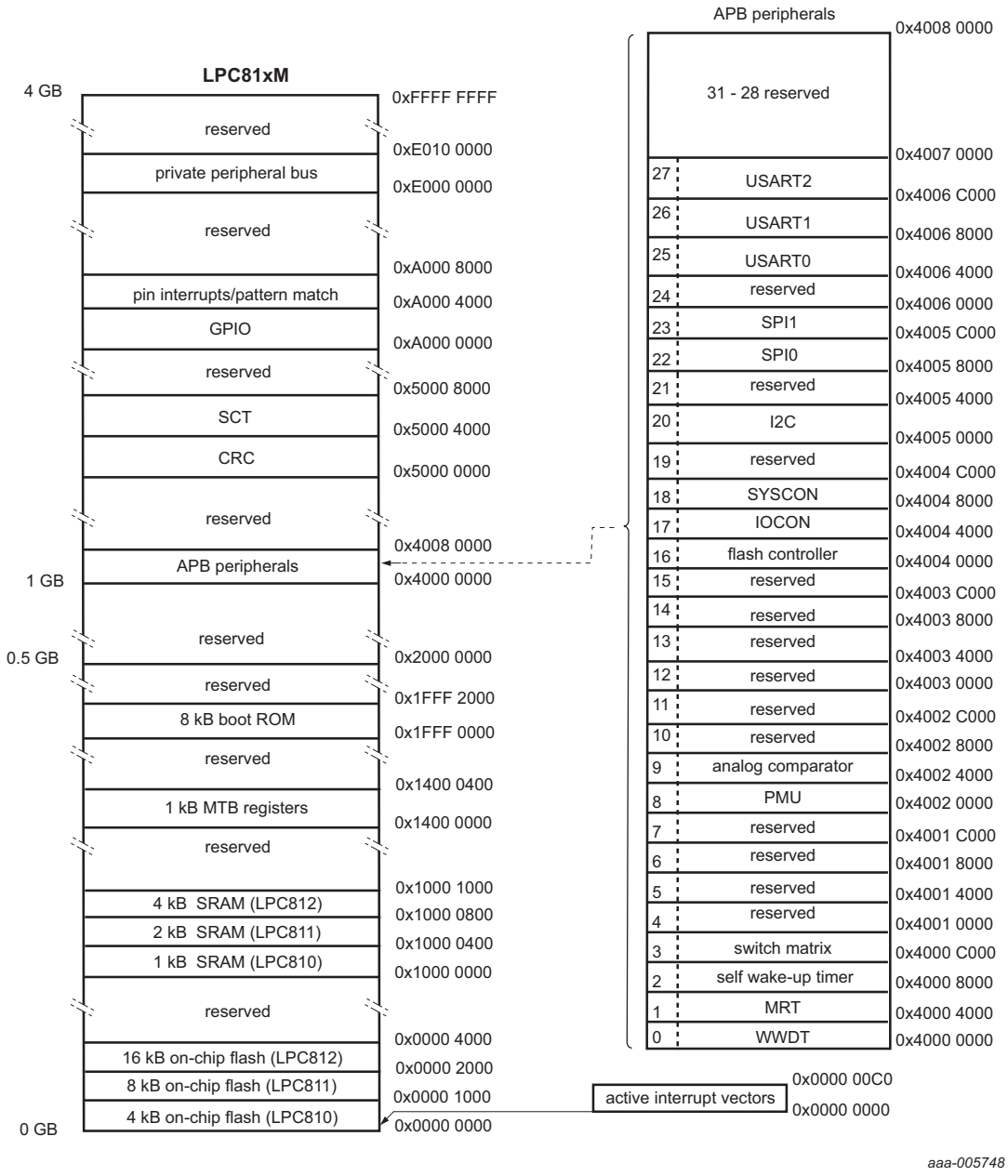
2.2.1 Memory mapping



The private peripheral bus includes the ARM Cortex-M0+ peripherals such as the NVIC, SysTick, and the core control registers.

Fig 2. LPC800 Memory mapping

2.2.2 Micro Trace Buffer (MTB)

The LPC800 supports the ARM Cortex-M0+ Micro Trace Buffer. See Section 26.5.4.