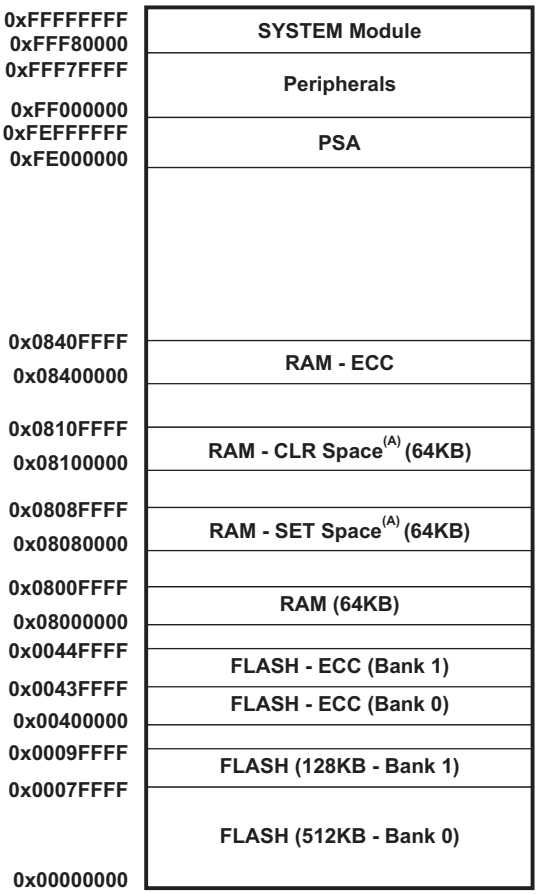
2.1 Memory Map Summary

2.1.1 Memory Map

Figure 2-1 shows the TMS470MF06607 memory map.



A. The RAM supports bit access operation which allows set/clear to dedicated bits without disturbing the other bits; for detailed description see the Architecture Specification.

Figure 2-1. TMS470MF06607 Memory Map

2.1.2 Memory Selects

Memories in the TMS470M devices are located at fixed addresses. Table 2-2 through Table 2-6 detail the mapping of the memory regions.

Table 2-2. TMS470MF06607-Specific Memory Frame Assignment

MEMORY FRAME NAME	START ADDRESS	ENDING ADDRESS	MEMORY TYPE	ACTUAL MEMORY
nCS0 (1)	0x0000 0000	0x0009 FFFF	Flash	640K Bytes
RAM-CLR	0x0810 0000	0x0810 FFFF	Internal RAM	64K Bytes
RAM-SET	0x0808 0000	0x0808 FFFF	Internal RAM	64K Bytes
CSRAM0 (1)	0x0800 0000	0x0800 FFFF	Internal RAM	64K Bytes
CSRAM0 (1)	0x0840 0000	0x0840 FFFF	Internal RAM-ECC	64K Bytes

(1) Additional address mirroring could be present resulting in invalid but addressable locations beyond those listed above. The device may generate an abort when accessing the unimplemented memory regions of peripheral memories. TI recommends the use of the MPU for protecting access to addresses outside the intended range of use.